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Mirko Loghi received the Dr.Eng. degree in electrical engineering from the University “La Sapienza” of Rome and the Ph.D degree in Computer Science from the University of Verona. In 2002 was employed in *Consorzio Ferrara Ricerche* and was a Visiting Researcher in SUN Microsystems at Menlo Park (CA-USA). From 2006 to 2008, he was a Postdoctoral Fellow at Politecnico di Torino, and he currently is an Assistant Professor at University of Udine.

His research interests mainly include neuromorphic computing, digital design, multiprocessor systems and architectural solutions for low-power.

M. Loghi is coauthor of papers on journals and peer-reviewed conferences and he was member of the TPC of international conferences (*VLSI-SoC* and *PARMA-DITAM*) and reviewer for international journals (“*IEEE Transactions on Computer-Aided Design*”, “*Integration: the VLSI Journal*”, “*IEEE Transactions on Design Automation of Electronic Systems*”, “*IEEE Transactions on VLSI*”, “*IEEE Transactions on Computers*”, “*IEEE Journal on Emerging and Selected Topics in Circuits and Systems*”) and conferences (*ACM/IEEE DAC*, *ACM/IEEE GLSVLSI*, *ACM/IEEE ISLPED*, *IEEE DATE*, *PATMOS*, *ACM/IEEE CASES*, *IEEE ISCAS*, *SASIMI*, *IEEE ICECS*).

He was involved in European projects “CLEAN” (FP6-2004-IST-4, *Controlling LEAKage power in NanoCMOS SoCs*), ARTEMIS-JU “nSHIELD” (New embedded Systems arcHitecturE for multi-Layer Dependable solutions), and “BeFerroSynaptic” (H2020-ICT-2019-2 GA nr. 871737, *BEOL technology platform based on ferroelectric synaptic devices for advanced neuromorphic processors*).

He was the lecturer of courses *Metodologie della sintesi logica*, *Calcolatori elettronici I*, *Calcolatori elettronici II*, and *Calcolatori elettronici e sistemi operativi* at University of Udine and is currently the lecturer of courses *Reti logiche e architetture dei calcolatori*, *Sistemi operativi*, and *Calcolatori elettronici* at University of Udine